Product Profile

SN74LVC1G14 is a Schmitt trigger function of the NOT gate integrated circuit, can realize mathematical logic operation. $Y = \overline{A}$ The chip is designed on an advanced CMOS process, featuring low power consumption and high output drive capability. The chip works well with a VCC supply voltage between 1.65 V and 5.5 V.The 74LVC1G14 is available in a variety of small package forms, which can be widely used in high-end precision instruments, miniaturized low-power handheld devices, and artificial intelligence.

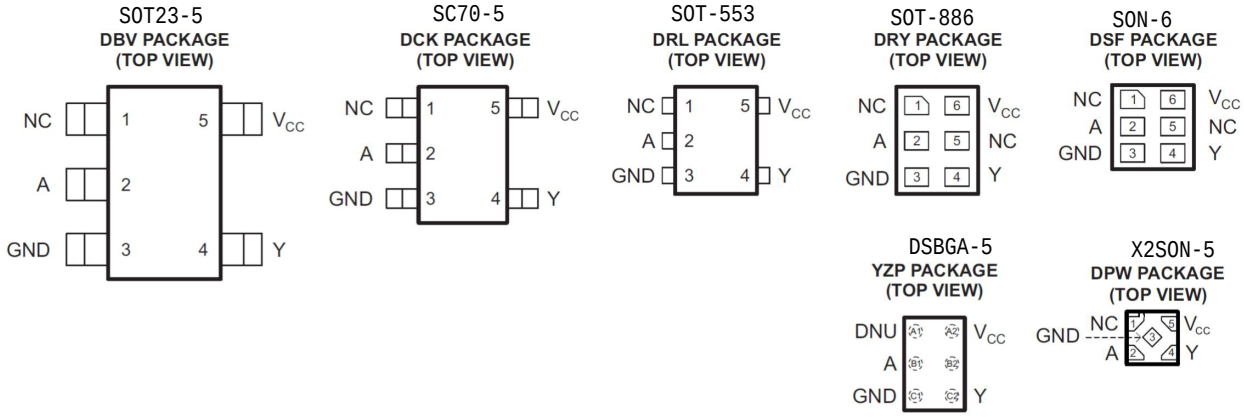
Product Features

- Low input current: 0.1 uA typical
- Wide operating range: 1.65 V to 5.5 V
- Low quiescent power consumption: 0.1 uA typical
- Package: DBV/ DCK/ DRL/ YZP/ DRY/ DSF/ DPW
- High output drive VCC = 4.5 V, greater than 32 MA

Product Usage

- Portable audio interface Blu-ray player and home theater
- Digital TV
- Solid state hard disk
- Intelligent wearable devices, such as wireless headphones, smart watches, etc.

Package form and pin function definition



	Pin				
Name	DBV/ DCK/ DRL	DRY/DSF	YZP	DPW	Description
NC	1	1,5	A1, B2	1	Empty foot
A	2	2	B1	2	Input
GND	3	3	C1	3	Power supply ground
Y	4	4	C2	4	Output
VCC	5	6	A2	5	Power supply positive

Note: NC null pin, no connecting wire inside.

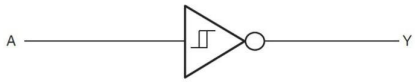
■ limiting parameter

Parameter	SYMBOLS	Limit value	Unit
Operating voltage	V_{CC}	6.5	V
Input	V_{IN}	-0.5 to 6.5	V
Output Voltage (1)	V_{OUT}	-0.5 to 6.5	V
Single pin output current	I_{OUT}	25	mA
Vcc or GND Current	I_{CC}	50	mA
Storage temperature	T_S	-65-150	℃
Lead Soldering Temperature	T_W	260,10s	℃

Note:1. Under VCC = 0V power-off state, the output can withstand the limit voltage.

2. The limit parameter refers to the limit value which cannot be exceeded under any condition.If this limit value is exceeded, physical damage such as product degradation may be caused; at the same time, near the limit parameters, it is impossible to guarantee that the chip can work normally.

■ Principle Logic Diagram



■ Truth Table

Inputs	Output
A	Y
L	H
H	L

■ Operating conditions

PROJECTS	SYMBOLS	Test Conditions	Min.	TYP	Max.	Unit
Operating voltage	V_{CC}	-	1.65	-	5.5	V
Input High Voltage	V_{IH}	V_{CC} =1.65V~1.95V	0.65* V_{CC}	-	-	V
		V_{CC} =2.3V~2.7V	1.7V	-	-	
		V_{CC} =3V~5.5V	0.7* V_{CC}	-	-	
Low-Level Input Voltage	V_{IL}	V_{CC} =1.65V~1.95V	-	-	0.35* V_{CC}	V
		V_{CC} =2.3V~2.7V	-	-	0.7	
		V_{CC} =3V~5.5V	-	-	0.3* V_{CC}	
Input Voltage	V_I	-	0	-	5.5	V
Output Voltage	V_O	-	0	-	V_{CC}	V
High Level Output Current	I_{OH}	V_{CC} =1.65V	-	-	-4	mA
		V_{CC} =2.3V	-	-	-8	
		V_{CC} =3V	-	-	-16	
		V_{CC} =4.5V	-	-	-32	
Low Level Output Current	I_{OL}	V_{CC} =1.65V	-	-	4	mA
		V_{CC} =2.3V	-	-	8	
		V_{CC} =3V	-	-	16	
		V_{CC} =4.5V	-	-	32	

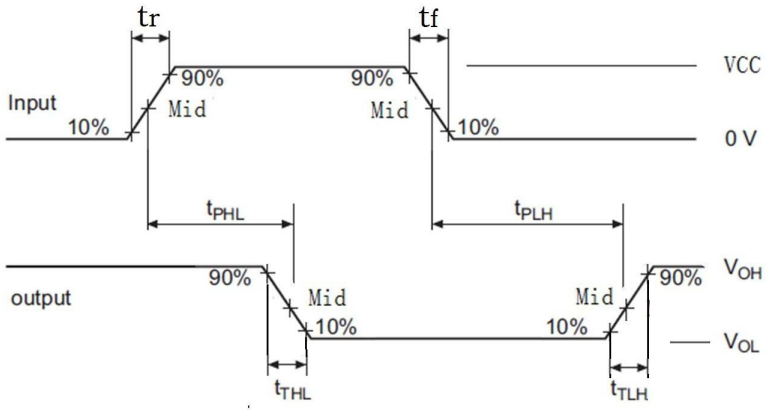
■ electrical characteristics

DC electrical characteristics: TA = 25 ℃

PROJECTS	SYMBOLS		Test Conditions	Vcc	TYP	Max.	Unit
Upper critical voltage	VT+		-	1.65V	1	-	V
				2.3V	1.35	-	
				3V	1.7	-	
				4.5V	2.5	-	
				5.5V	3	-	
lower critical voltage	VT-		-	1.65V	0.5	-	V
				2.3V	0.7	-	
				3V	1.1	-	
				4.5V	1.65	-	
				5.5V	1.9	-	
Hysteresis Width Voltage	Δ V_T (VT+ - VT-)		-	1.65V	0.5	-	V
				2.3V	0.65	-	
				3V	0.6	-	
				4.5V	0.85	-	
				5.5V	1.1	-	
High level load voltage	V_{OH}		I_{OH} = -100 uA	1.65V~5.5V	1.64	-	V
			I_{OH} = -4 mA	1.65V	1.47	-	
			I_{OH} = -8mA	2.3V	2.15	-	
			I_{OH} = -16 mA	3V	2.73	-	
			I_{OH} = -32 mA	4.5V	4.0		
Low Level Load Voltage	V_{OL}		I_{OH} = 100 uA	1.65V~5.5V	0.01	-	V
			I_{OH} = 4 mA	1.65V	0.11	-	
			I_{OH} = 8 mA	2.3V	0.11	-	
			I_{OH} = 16 mA	3V	0.2	-	
			I_{OH} = 32 mA	4.5V	0.35	-	
Input Current	I_I	A	V_I = 5.5V or GND	0~5.5V	0.01	± 5	uA
Shutdown Current	I_{OFF}	V_I	V_I = 5.5V	0	0.01	± 10	uA
		V_O	V_O = 5.5V	0	0.01	± 10	
Operating current	I_{CC}		V_I = 5.5 V, I_O = 0	1.65V~5.5V	0.01	10	uA
			V_I = GND, I_O = 0		0.01	10	
Operating current variation value	ΔI_{CC}		A=V_{CC} -0.6V	3V~5.5V	25	-	uA

AC electrical characteristics: Ta = 25 ℃ Vcc = 5.0V, tr = tf ≤ 20ns, see test method.

PROJECTS	SYMBOLS	Test Conditions	Min.	TYP	Max.	Unit
Maximum transmission delay time A,B to Y	t_{PHL}	C_L = 15 pF	-	20	-	ns
	t_{PLH}	C_L = 15 pF	-	20	-	ns



Note:1. The CL capacitor is an external patch capacitor (0603), which is connected near the output pin, and the capacitor ground is close to chip GND;

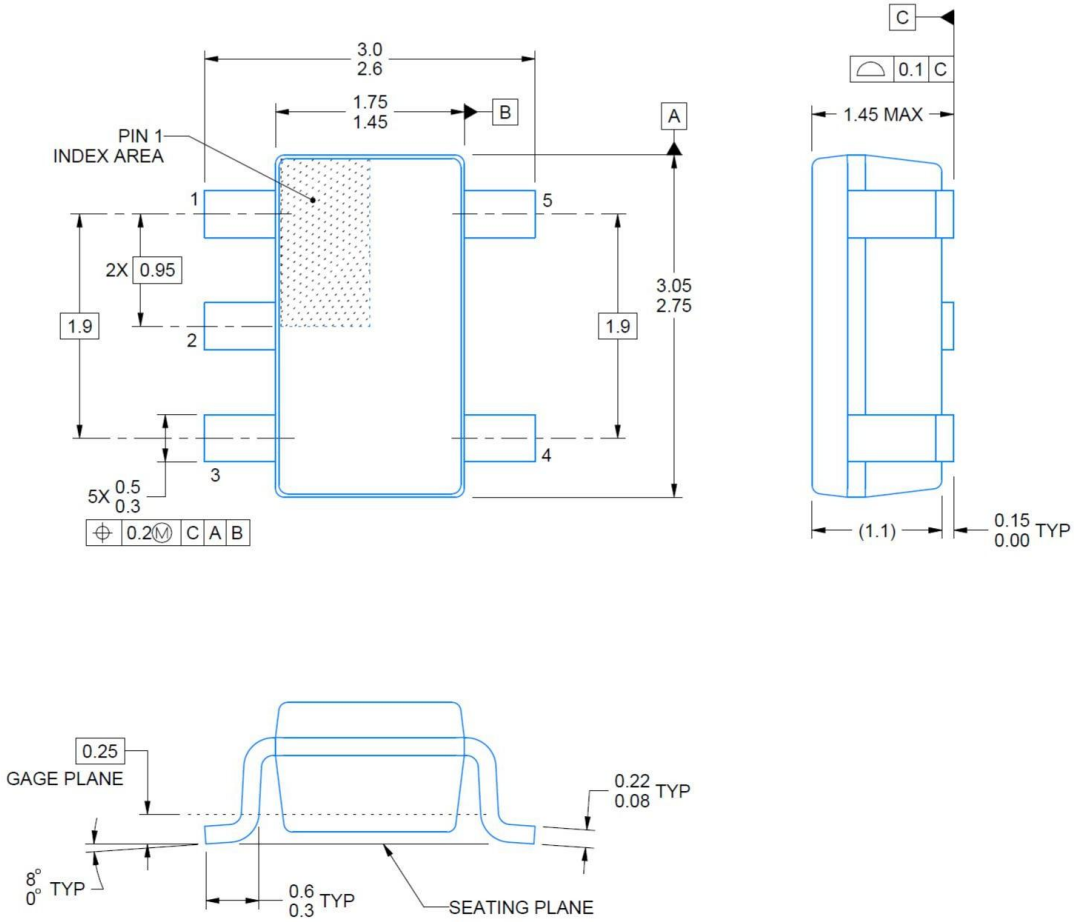
2、Input: port input level, f = 500 kHz, D = 50%; tr = tf ≤ 20 ns;

3、Output: Y-Terminal Output Test.

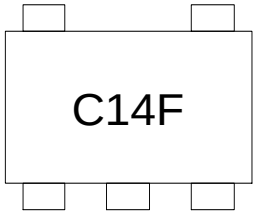
■ Package Information

Unit: mm/ inch

DBV (SOT23-5)

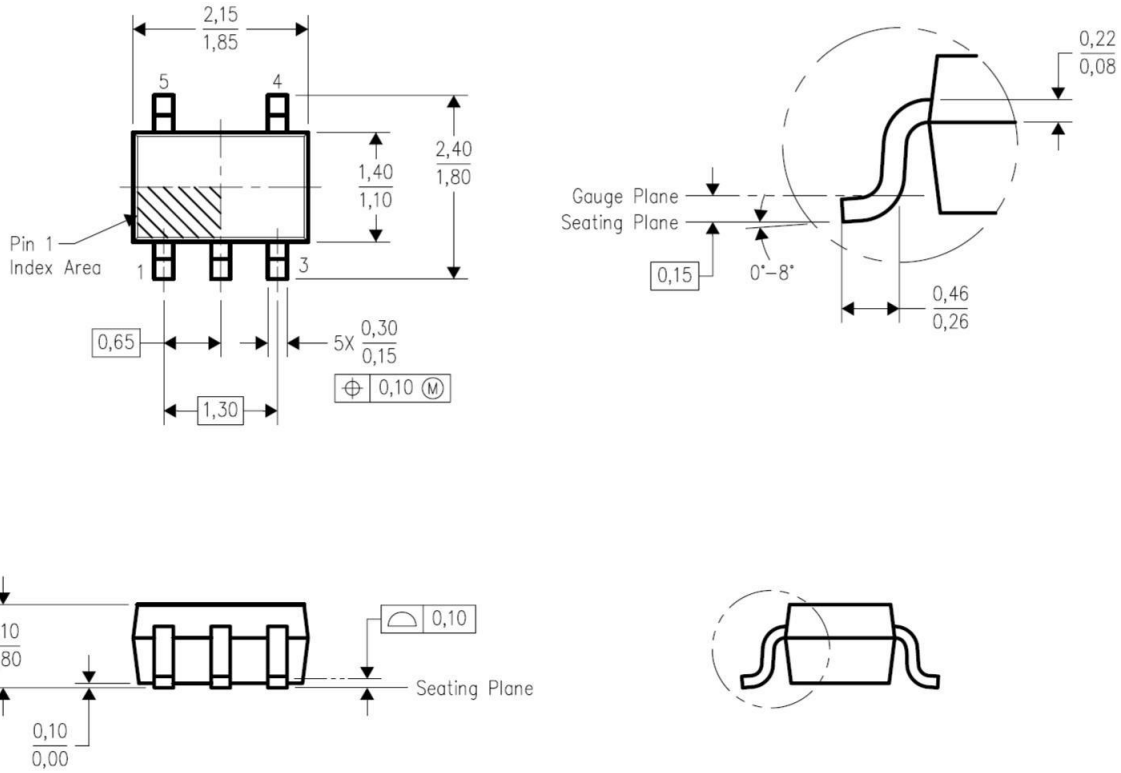


■ Marking



■ Package Information

DCK (SC70-5)



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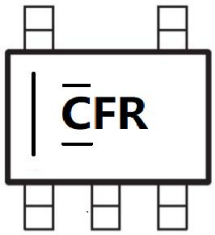
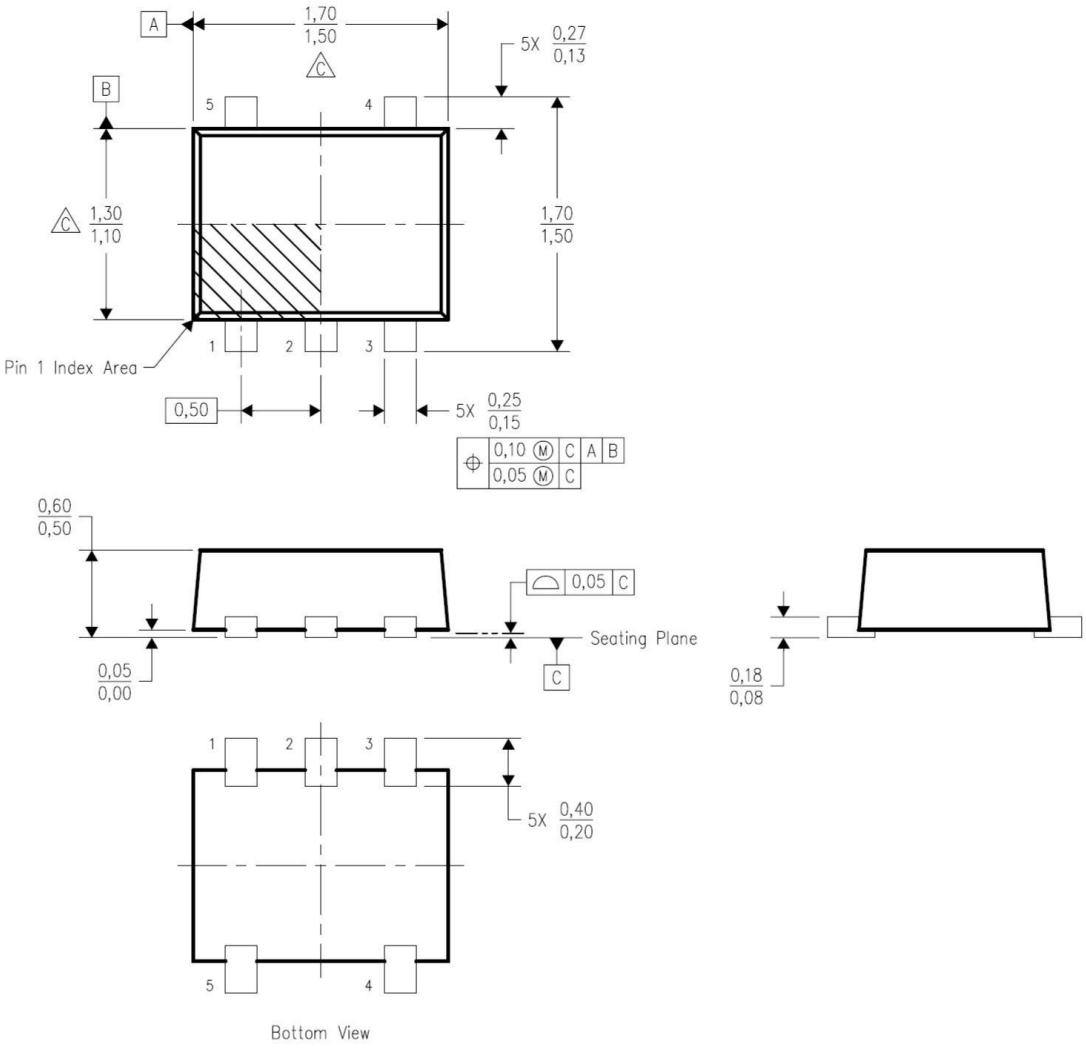
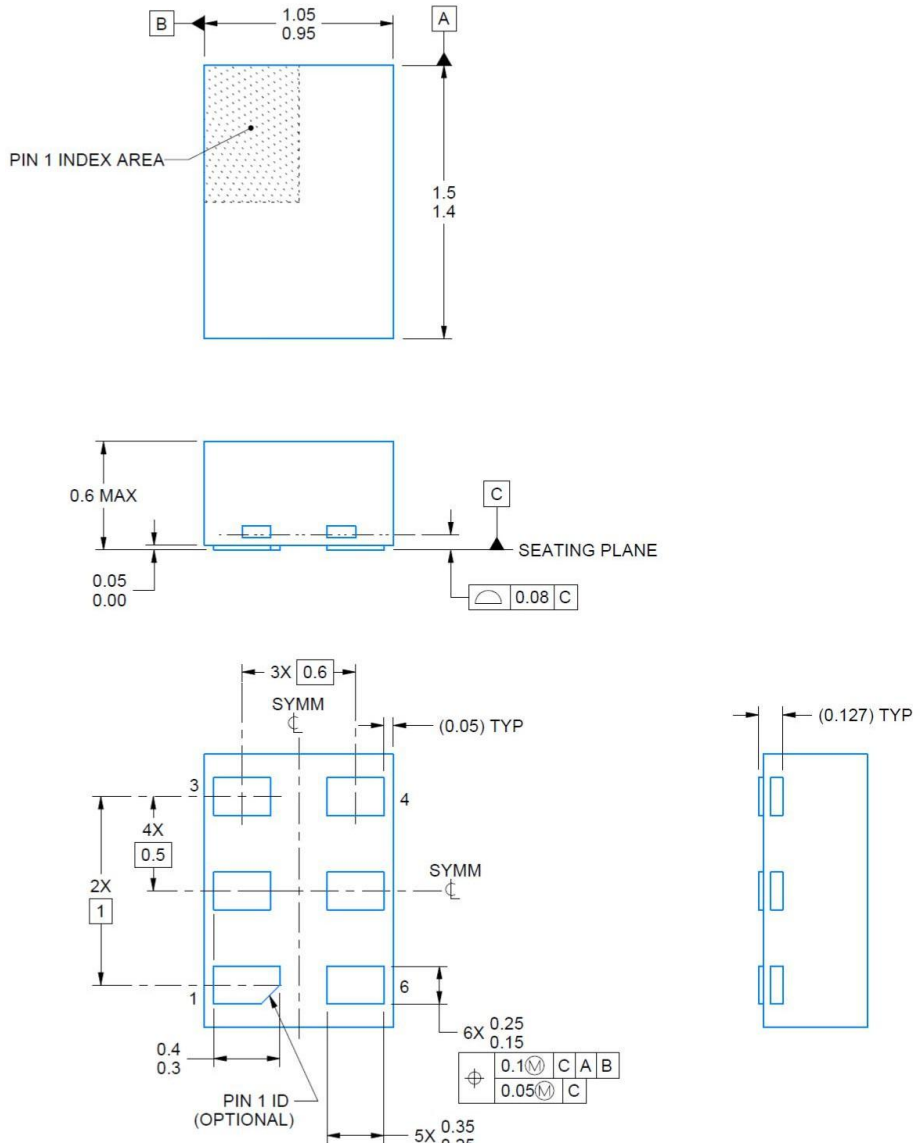


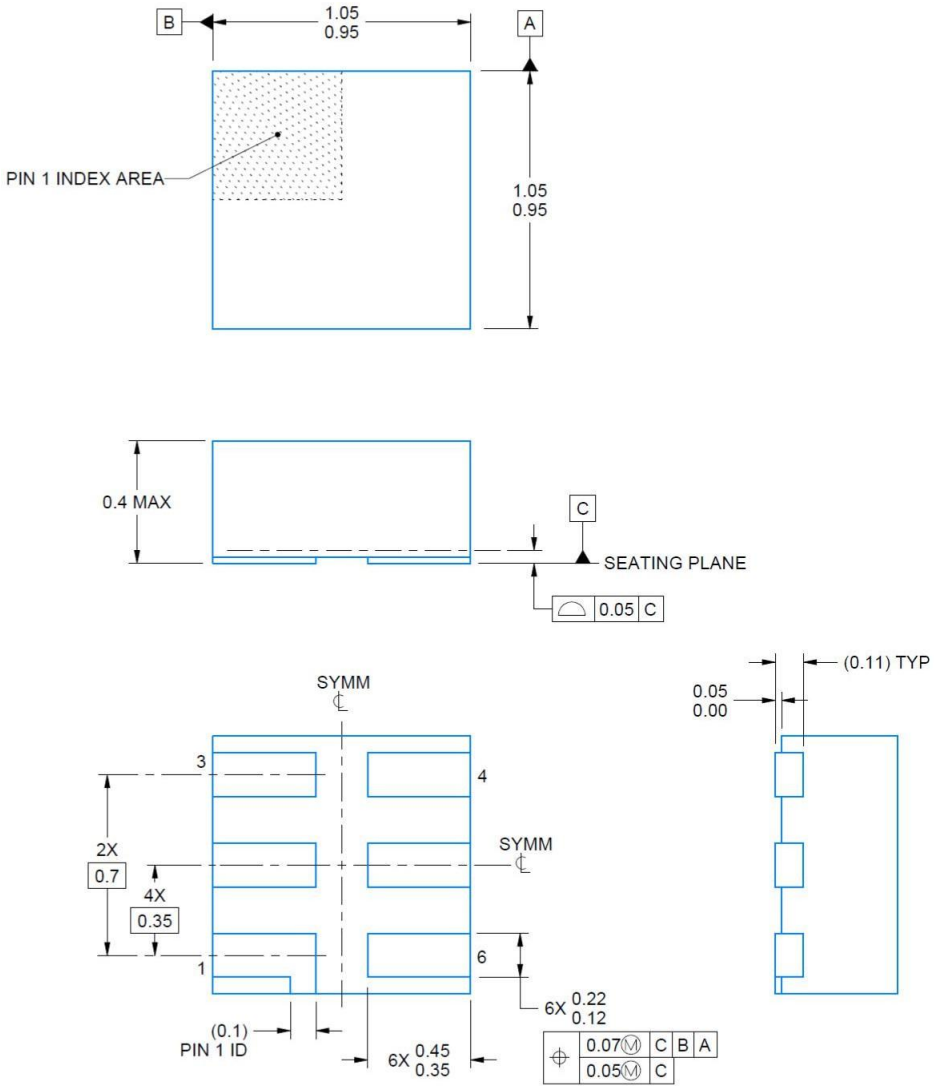
DRL(SOT-553)


A
1,70
1,50
C
5X 0,27
0,13
B
5
4
C
1,30
1,10
1,70
1,50
1
2
3
Pin 1 Index Area
0,50
5X 0,25
0,15
0,10 M C A B
0,05 M C
0,60
0,50
0,05 C
Seating Plane
C
0,05
0,00
0,18
0,08
1
2
3
5X 0,40
0,20
5
4
Bottom View

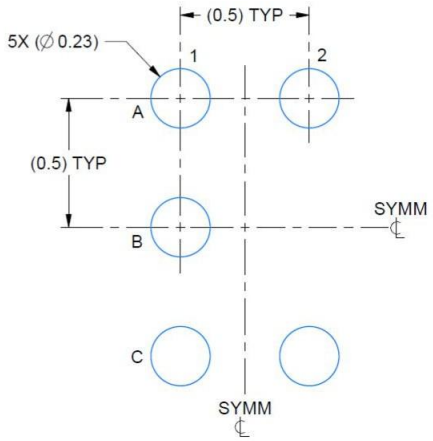
DRY(SOT-886)


B
1.05
0.95
A
PIN 1 INDEX AREA
1.5
1.4
0.6 MAX
C
SEATING PLANE
0.05
0.00
0.08 C
3X 0.6
SYMM
(0.05) TYP
(0.127) TYP
3
4
4X
0.5
SYMM
2X
1
1
6
6X 0.25
0.15
0.1 C A B
0.05 C
0.4
0.3
PIN 1 ID
(OPTIONAL)
5X 0.35

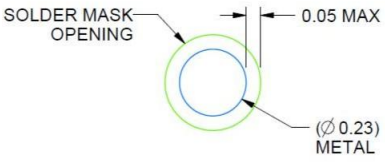
DSF(SON-6)


B
1.05
0.95
A
PIN 1 INDEX AREA
1.05
0.95
0.4 MAX
C
SEATING PLANE
0.05 C
SYMM
(0.11) TYP
0.05
0.00
3
4
2X
0.7
4X
0.35
SYMM
1
6
6X 0.22
0.12
(0.1)
PIN 1 ID
6X 0.45
0.35
0.07 M C B A
0.05 M C

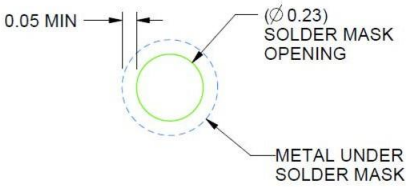
YZP(DSBGA-5)



LAND PATTERN EXAMPLE
SCALE:40X

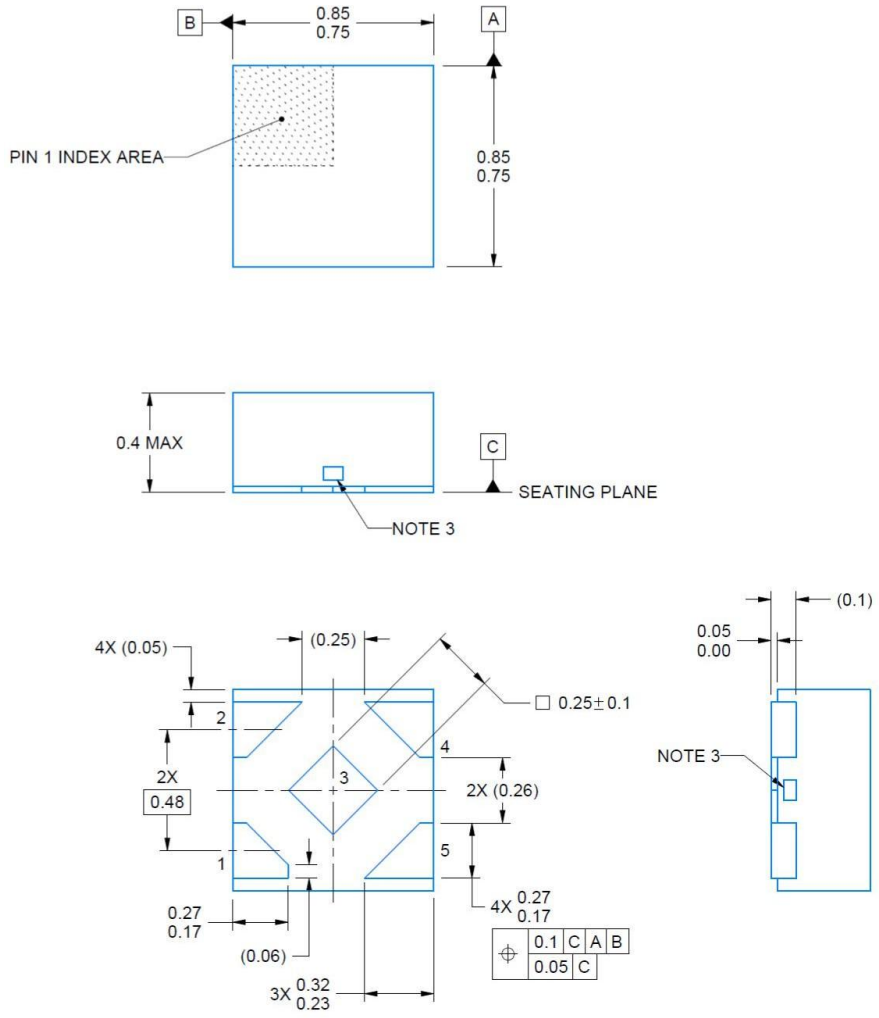


NON-SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

DPW(X2SON-5)



Ordering information

Order code	Package	Baseqty	Deliverymode
SN74LVC1G14DBVR	SOT23-5	3000	Tape and reel
SN74LVC1G14DCKR	SC70-5	3000	Tape and reel
SN74LVC1G14DSFR	SON-6	5000	Tape and reel
SN74LVC1G14DRYR	SOT-886	5000	Tape and reel
SN74LVC1G14YZPR	DSBGA-5	3000	Tape and reel
SN74LVC1G14DPWR	X2SON-5	3000	Tape and reel
SN74LVC1G14DRLR	SOT-553	4000	Tape and reel